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FOR

ARRAY CAPACITORS WITH VOIDS TO ENABLE A FULL-GRID SOCKET

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ARRAY CAPACITORS WITH VOIDS TO ENABLE A FULL-GRID SOCKET

BACKGROUND

Field

[0001] Embodiments of the invention relate to capacitors and integrated circuit (IC) package assembly, and more specifically, to array capacitors suitable for use with integrated circuits mounted on IC packages.

Background

[0002] Typically, in integrated circuit (IC) packages such as for mounting IC dies, among other integrated circuitry, a voltage regulator circuit is used to provide electrical power to the semiconductor die. One way of providing voltage regulation to an IC die or chip is mounting a voltage regulator module (VRM) on a printed circuit board (PCB), for example, of a computer system. However, the VRM by itself cannot meet all the power demands of high-speed microelectronic devices (e.g., high performance processors). Specifically, the VRM cannot respond immediately to sudden changes in the current drawn by the die which could generate unacceptably large reductions in voltage, often called voltage droops. This voltage drop on the die increases the switching time of the transistors on the die, which degrades the performance of the system fabricated on the die. To ameliorate excessive voltage droops, decoupling capacitors may be used to assist in preventing a drop in voltage levels in an IC die.

[0003] Discrete decoupling capacitors are typically mounted adjacent to the IC die and connected to the conductors that provide power to the die. For a processor die, the die may be mounted on a substrate (e.g., an IC package), and a number of discrete capacitors may be mounted on the substrate along the periphery of the die and/or underneath the die. These capacitors are coupled to the power supply connections at the die through lands formed on the substrate. The capacitors may be used to store energy for use by the die during periods of non-steady state or transient current demands, or to manage noise problems that occur in the die.

[0004] One concern associated with power decoupling is inductance in the path from the chip (IC die) to the capacitors. As the chips get faster, it is critical to keep this inductance small in order to manage the high frequency noise. In order to minimize the effective inductance in the path from the chip to the capacitors, the capacitors are typically placed on the backside of the package under the die shadow. In order to accommodate these capacitors, the sockets that are used in microprocessors today have a cavity in the center.

[0005] While the capacitors on the package take care of the high frequency noise, they do not have enough capacitance to address the low frequency noise. A significant contribution to the low frequency noise comes from the resistance in the path from the VRM to the chip. This is comprised of the motherboard (MB) resistance, the socket resistance and the package resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which like references indicate similar elements. It should be noted that the references to “an” or “one” embodiment of this disclosure are not necessarily to the same embodiment, and such references mean at least one.

[0007] Figure 1 shows a cross-sectional side elevational view of an array capacitor for a package assembly according to one embodiment.

[0008] Figure 2 shows an enlarged side elevation view of a portion of the package assembly 100 shown in Figure 1.

[0009] Figure 3 shows a cross-sectional side elevational view of a portion of an array capacitor according to one embodiment.

[0010] Figure 4 shows a top plan view of an internal structure of an array capacitor according to one embodiment.

[0011] Figure 5 shows a flowchart diagram illustrating a process of incorporating an array capacitor into an integrated circuit package according to one embodiment.

DETAILED DESCRIPTION

[0012] In the following description, specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail to avoid obscuring the understanding of this description.

[0013] Figure 1 shows a cross-sectional side elevational view of an array capacitor for a package assembly according to one embodiment. The package assembly includes an integrated circuit (IC) 110, which is housed by IC package 120. The integrated circuit 110 may contain one or more circuits that are electrically connected to the package 120 by connectors 115. In one embodiment, the connectors 115 are bump (solder ball) type electrodes. These circuits may act as the intended load to which power is supplied by the VRM through the package. Although not shown herein, a voltage regulated power supply which may be provided in a VRM of a known type may be mounted on a printed circuit board (PCB) 130, such as a motherboard.

[0014] Integrated circuit 110 may be a high-speed processor, which may be employed in computers, servers or network systems or otherwise and may be other types of circuits. In one embodiment, the integrated circuit 110 may be a semiconductor die or may be representative of one or more IC chips or a combination of different types of circuits including high-performance dies or chips, although not limited thereto. In the illustrated embodiment, an IC die 110 is shown which has bumps 115 (e.g., solder balls) mounted 115 on an upper surface of IC package 120. Alternatively, the integrated circuit 110 may be a surface mounted chip, in which input/output terminals thereof are connected to the IC package 120 using bond wires for connecting the chip to bonding pads at the upper surface of IC package 120. Although not shown herein, embedded capacitors may be incorporated within the integrated circuit 110 and/or the IC package 120, as deemed necessary.

[0015] Also included within the package assembly 100 is an array capacitor 140. In an embodiment, the array capacitor 140 is placed on the backside of the IC package 120 underneath the integrated circuit 110. IC package 120, in Figure 1, is coupled to a socket 125, which is on the PCB 130. As shown in Figure 1, the pins from the package, including pins passing through the array capacitor, are inserted into the socket. In one embodiment, the socket 125 is configured to receive power and ground pins extending from the backside of the package under the die shadow. The socket 125 is shaped to accommodate the array capacitor 140. In an embodiment, a portion of the socket 125 located underneath the integrated circuit 110 is recessed to make room for the array capacitor 140.

[0016] In one embodiment, the socket and package resistance is reduced by using a full-grid socket 125 with no cavity and adding power and ground pins 135 on the backside of the package under the die shadow. More specifically, because the power and ground pins 135 located directly underneath the integrated circuit (e.g., semiconductor die) 110 are allowed to pass through the array capacitor 140, this arrangement enables a low resistance path through the array capacitor.

[0017] Figure 2 shows an enlarged side elevation view of a portion of the package assembly 100 shown in Figure 1. A portion of an array capacitor 140 is illustrated in Figure 2, which has voids or openings 155 to enable pins 135 from the IC package 120 to pass through. In an embodiment, the diameter of each void or opening 155 formed in the array capacitor 140 is slightly greater than the diameter of each pin 135 from the IC package 120 such that a defined distance 160 is maintained between the edge of the opening and the pin.

[0018] In the illustrated embodiment, the array capacitor includes a number of first conductive layers 201, 203, 205, 207 and 209 interleaved with a number of second conductive layers 202, 204, 206, 208 and 210. Dielectric layers 211 through 220 separate adjacent conductive layers. The first conductive layers 201, 203, 205, 207 and 209 are configured to be coupled to a first node in a circuit. In an embodiment, the first node is a ground plane 230 provided in the IC package 120. The second conductive layers 201, 203, 205, 207 and 209 are configured to be coupled to a second node in a circuit. In an embodiment, the second node is a power plane 235 provided in the IC

package 120. The power plane 235 provides a positive potential to the second conductive layers. In an embodiment, the ground plane 230 and the power plane 235 are coupled to the integrated circuit 110 (e.g., semiconductor die) to provide electrical power and grounding to the circuits contained in the die.

[0019] In an embodiment, the array capacitor 140 is electrically coupled to the ground plane 230 and the power plane 235 in the package 120 via bumps 150 (e.g., solder balls) provided between the array capacitor 140 and the package 120. While the illustrated array capacitor 140 is shown with ten layers 201 through 210, it should be noted that the number of layers may be greater than ten in an embodiment. In another embodiment, the number of layers is less than ten. Capacitance may be determined by the surface area of the plates and the distance between the plates, generally the greater the surface area, smaller the distance between the plates and/or greater the dielectric constant, the greater the capacitance.

[0020] Figure 3 shows a cross-sectional side elevational view of a portion of an array capacitor according to one embodiment. The array capacitor 140 includes a main body 305 having a top surface 310 and a bottom surface 315. In an embodiment, the top surface 310 and the bottom surface 315 have a substantially square and rectangular shape. It should be noted that other shapes such as circular or oval may be used with the capacitors described herein.

[0021] The array capacitor 140 includes a number of first conductive vias 331, 333, 335, 337, 339, 343 to electrically connect the first conductive layers 201, 203, 205, 207, 209 and a number of second conductive vias 334, 336, 338, 340, 342 to electrically connect the second conductive layers 202, 204, 206, 208, 210. In an embodiment, the first conductive vias 331, 333, 335, 337, 339, 343 are used to electrically connect the first conductive layers 201, 203, 205, 207, 209 to a ground plane in the IC package via first conductive terminals (e.g., solder balls) 351, 353, 355, 357, 359, 353, respectively. In an embodiment, the second conductive vias 334, 336, 338, 340, 342 are used to electrically connect the second conductive layers 202, 204, 206, 208, 210 to a power plane in the IC package via first conductive terminals (e.g., solder balls) 354, 356, 358, 360, 362, respectively. The array capacitor 140 further includes a number of openings 371, 372, 373 that extend vertically between the top

surface 310 and the bottom surface 315 of the main body 305. The openings 371, 372, 373 are sized and shaped to enable pins from an IC package to pass through.

[0022] Figure 4 shows a plane view of an array capacitor according to one embodiment. Specifically, Figure 4 shows a section surface on which a second conductive layer 202 is disposed. The first conductive vias 331, 333, 335 pass through the second conductive layer 202, which form gaps 401, 403, 405 around the part where the first conductive vias 331, 333, 335 pass through. In an embodiment, the first conductive vias 331, 333, 335 are insulated from the second conductive layer 202. The second conductive layer 202 is connected to other second conductive layers by the second conductive vias 334, 336.

[0023] Also illustrated in Figure 4 are a number of pin-insertable openings 371, 372, 411, 412 formed in the array capacitor 140. In an embodiment, the number of and the spacing between the pin-insertable openings are selected to accommodate pins from the package extending from the location of the array capacitor. The illustrated array capacitor is shown with four pin-insertable openings. However, it should be noted that the number of pin-insertable openings may be greater than four in an embodiment. In another embodiment, the number of openings is less than four.

[0024] Figure 5 shows a process of incorporating an array capacitor into an integrated circuit package according to one embodiment. In block 510, an array capacitor with voids is provided. This may be done by fabricating a complete array capacitor and then forming voids or holes in the array capacitor subsequent to the fabrication of the array capacitor. The voids or holes formed in the array capacitor are arranged to coincide with the pins extending from the IC package. Then in block 520, an integrated circuit housed by an IC package is provided. The array capacitor is positioned with respect to the IC package by passing the IC package pins through the openings formed in the array capacitor such that the array capacitor is located directly underneath the integrated circuit mounted on the IC package (block 530). Then, the array capacitor is electrically connected to the IC package by using the conductive terminals provided on the array capacitor to couple with the ground plane and power plane provided in the IC package (block 540). Then in block 550, the IC package and the array capacitor is connected to a socket on a printed circuit board.

[0025] It should be noted that because embodiments of the capacitors described herein are capable of being mounted to an IC package directly underneath the semiconductor die and has openings to enables pins located directly underneath the die to pass through, the package resistance can be reduced without sacrificing the package decoupling performance. In one embodiment, the capacitor described herein is used to satisfy high frequency noise and low frequency noise requirements of high-performance processors.

[0026] While several embodiments have been described, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.